

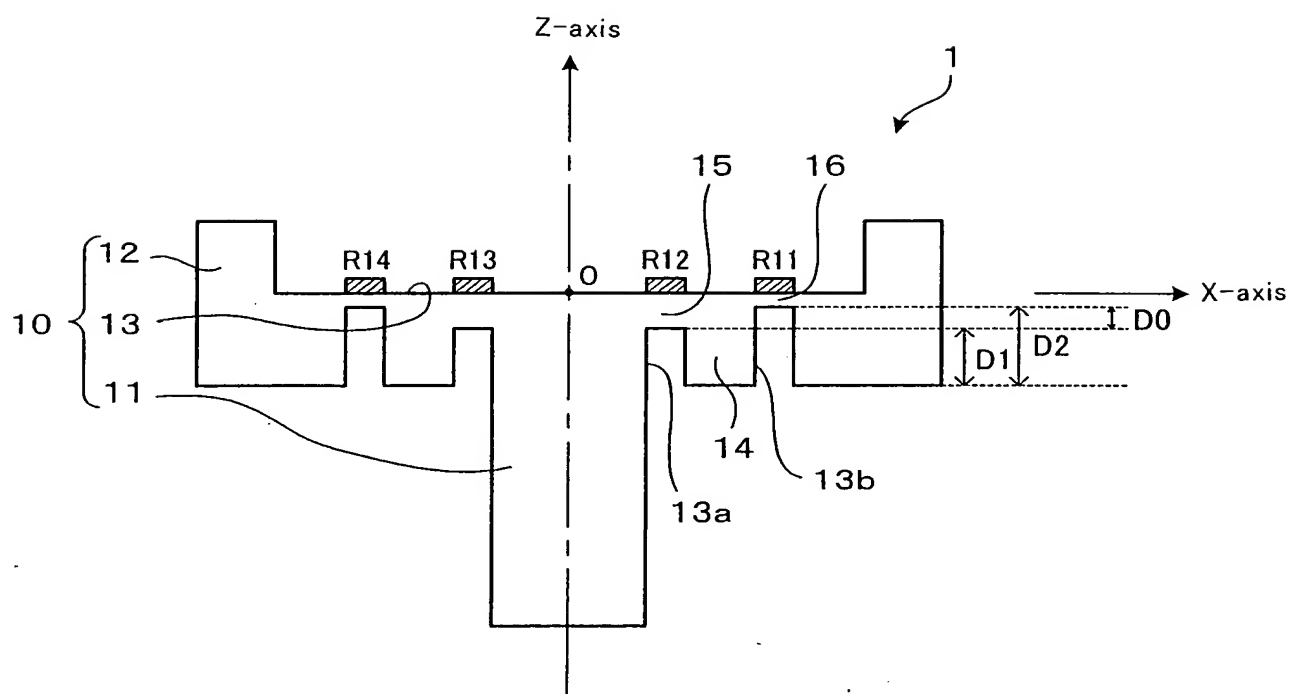
[illegible]

FIG. 2

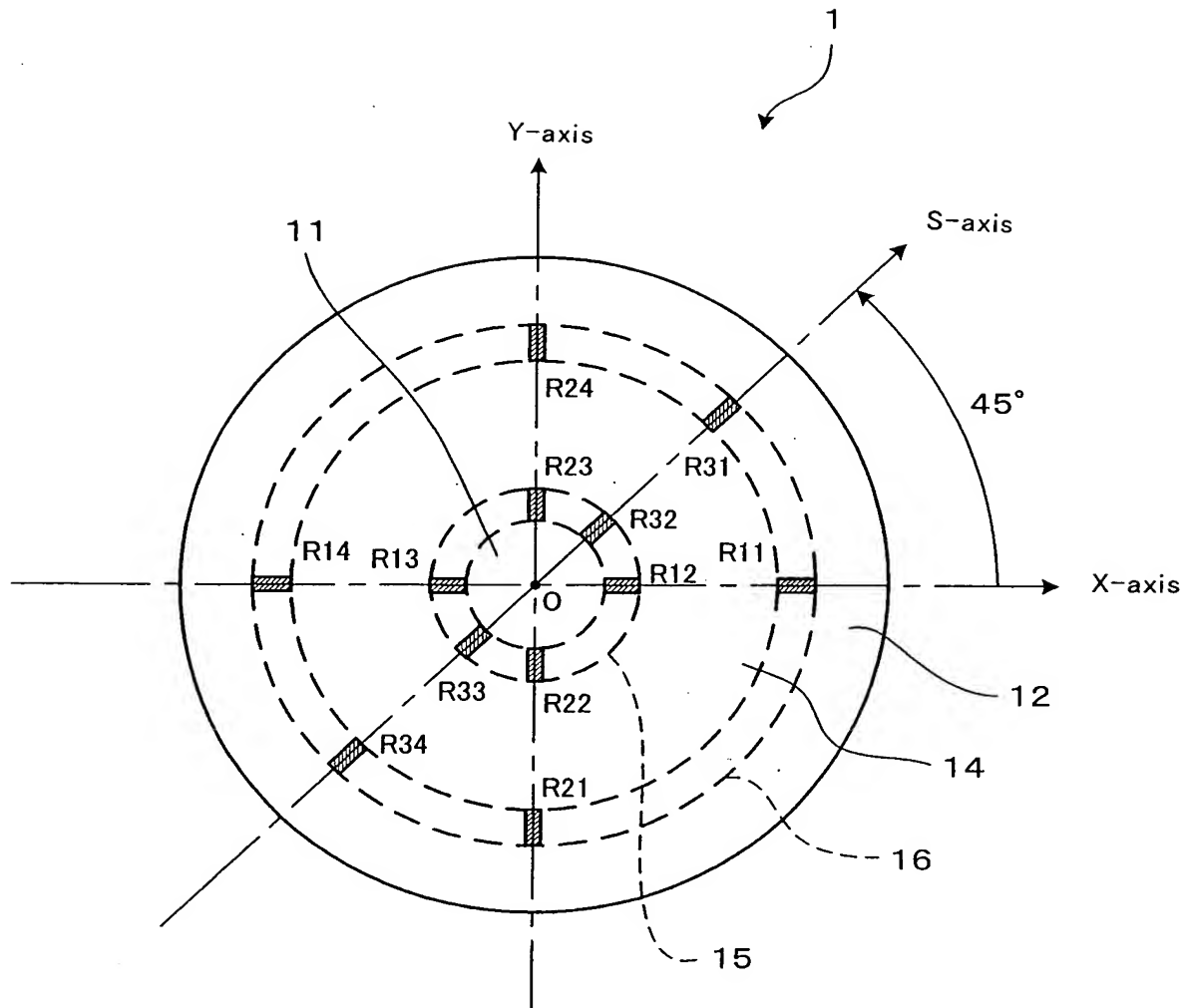


FIG. 3

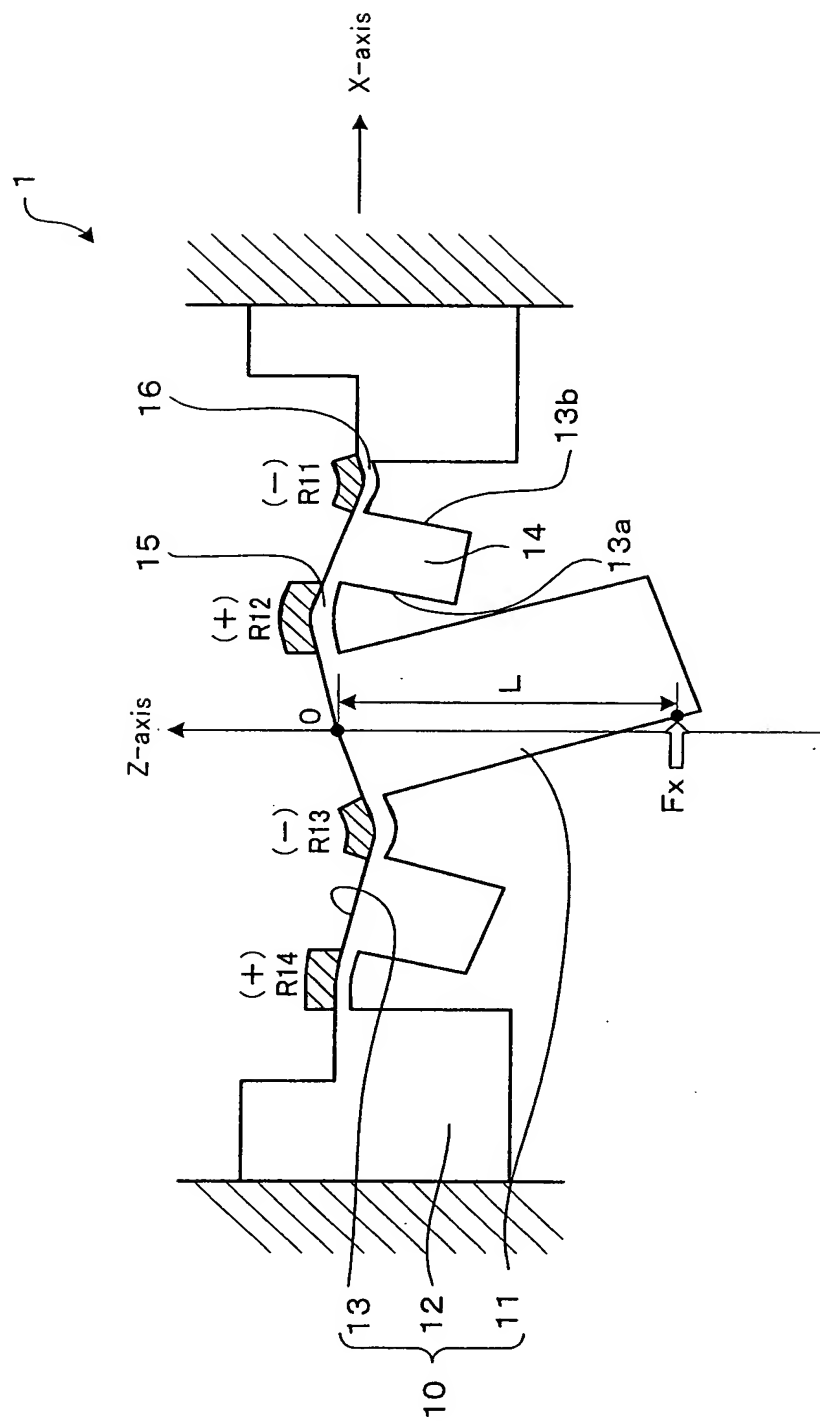


FIG. 4

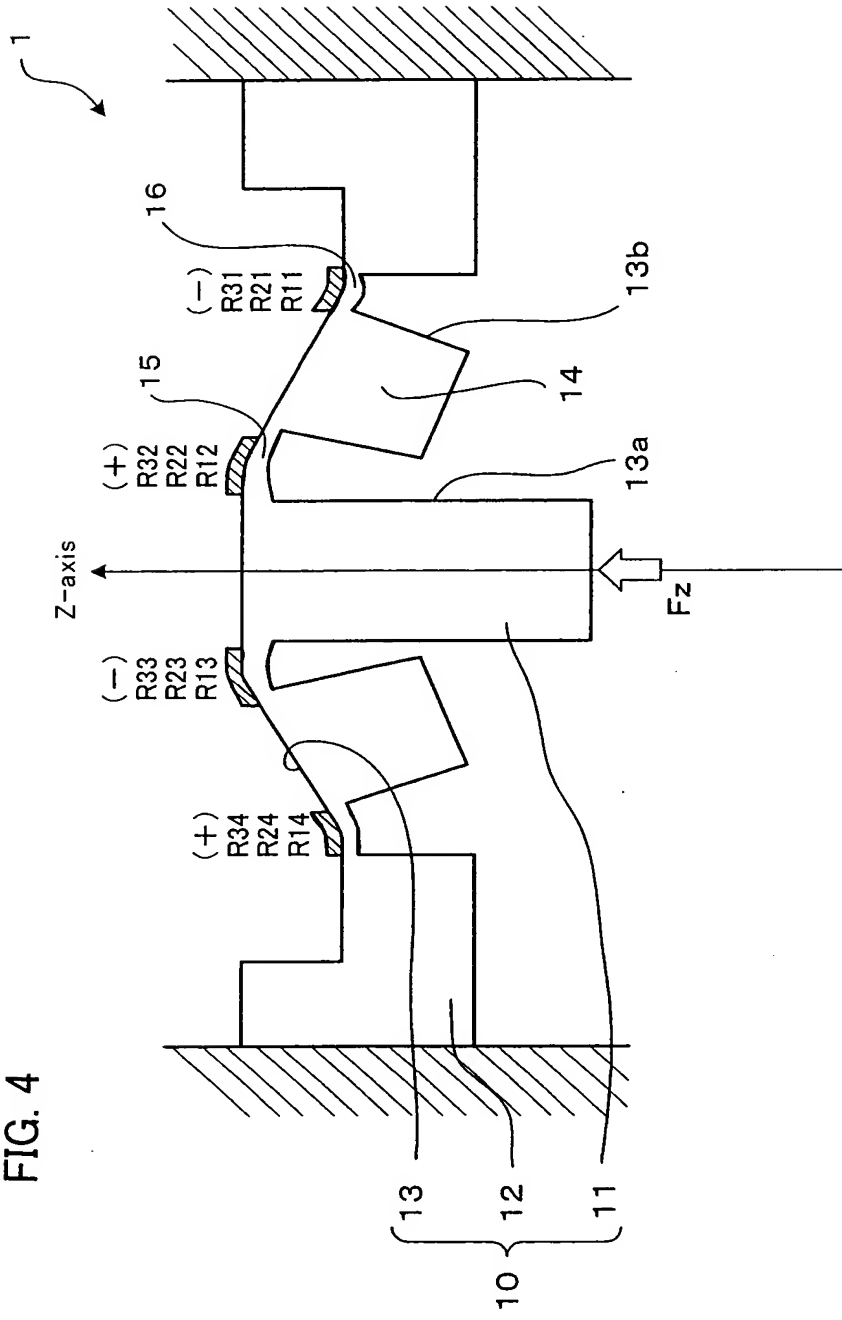


FIG. 5A

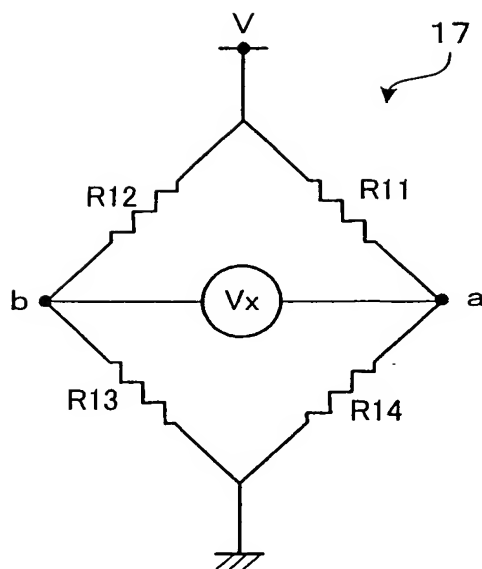


FIG. 5B

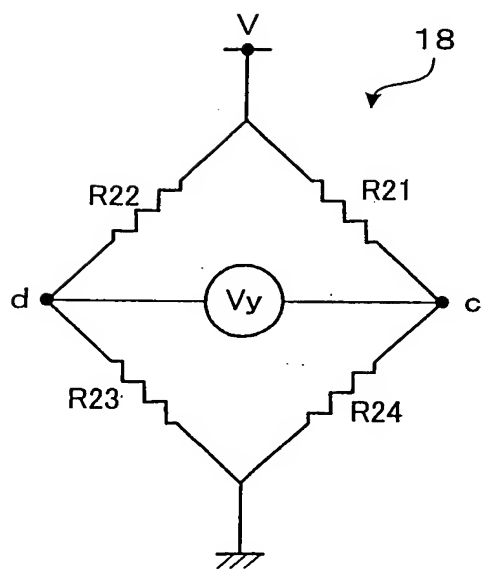


FIG. 5C

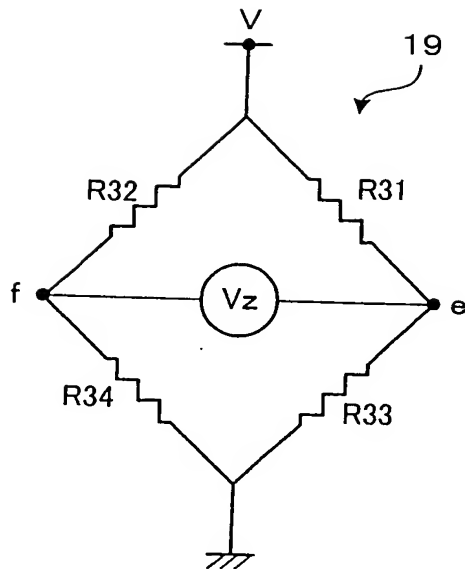


FIG. 6

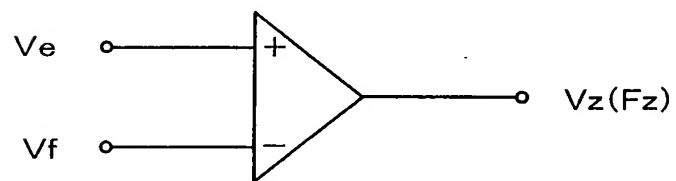
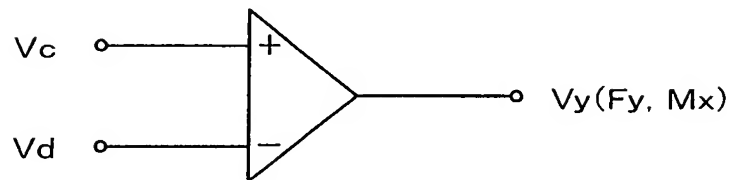
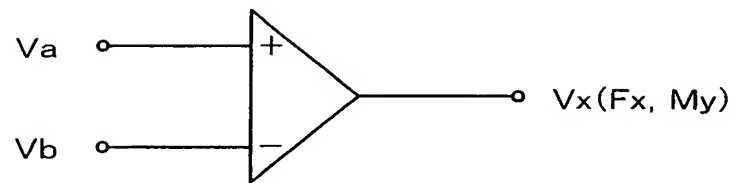


FIG. 7

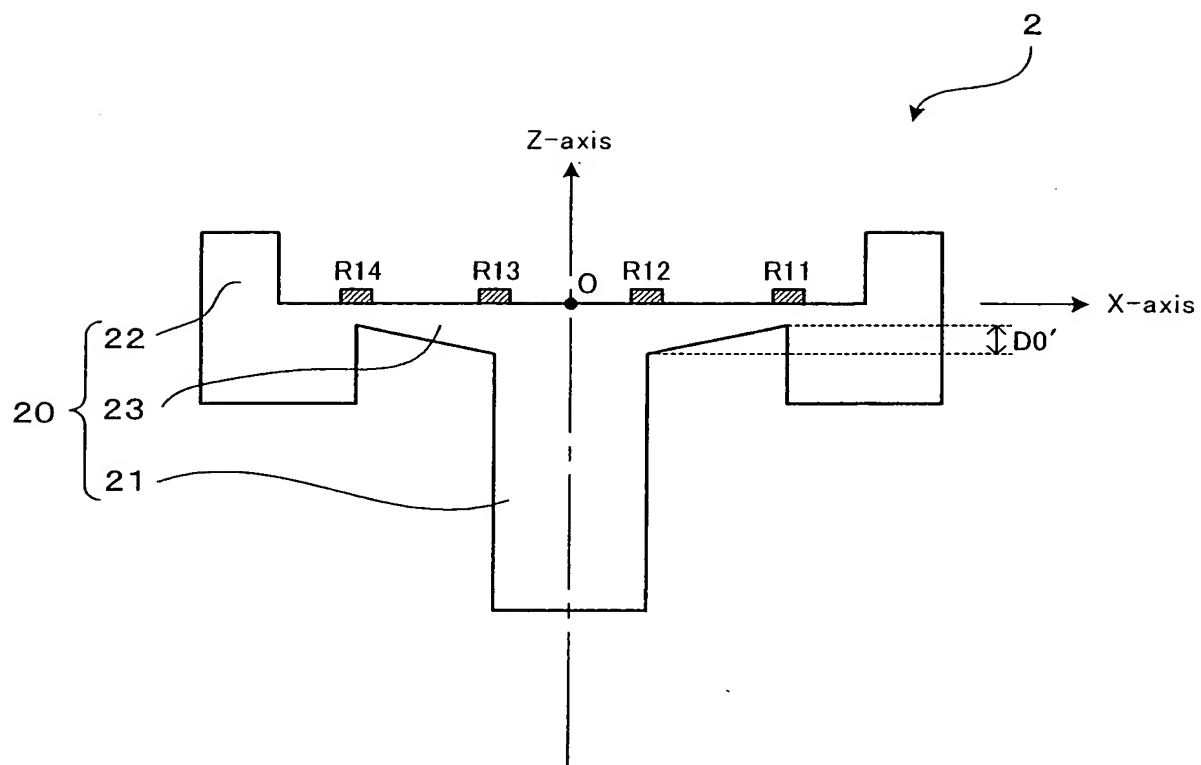




FIG. 8

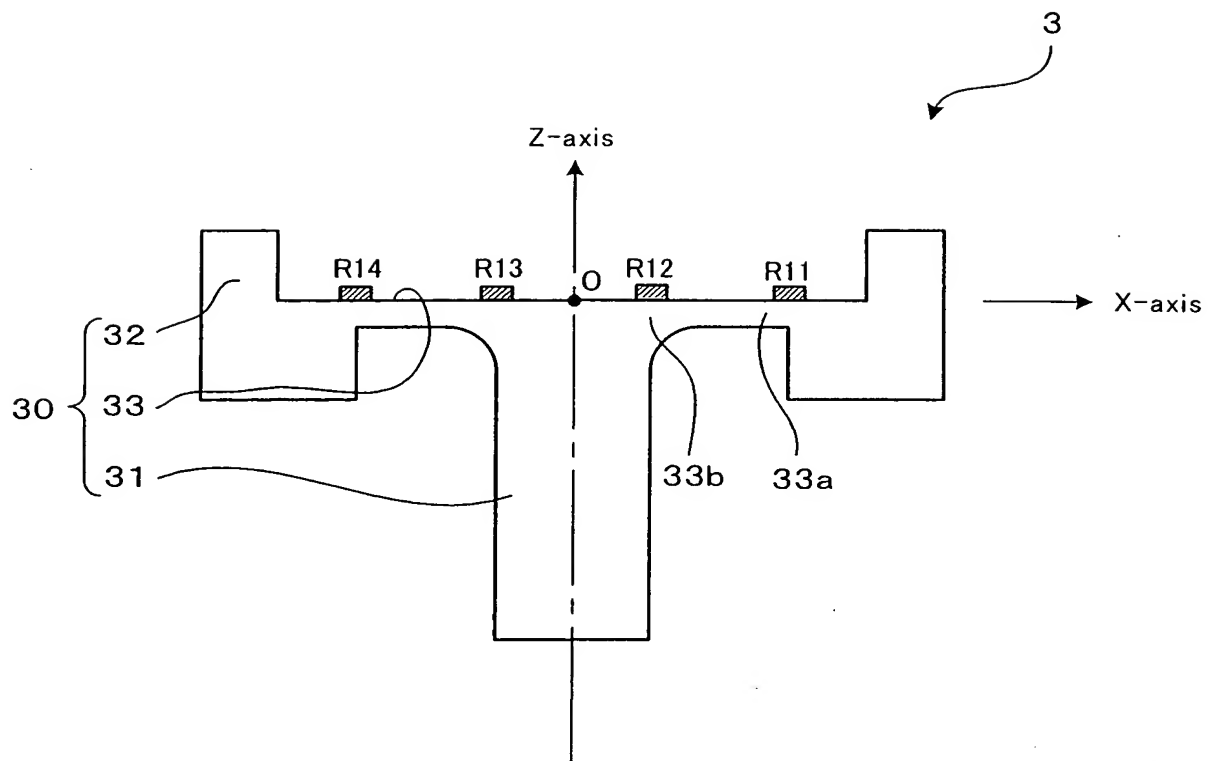
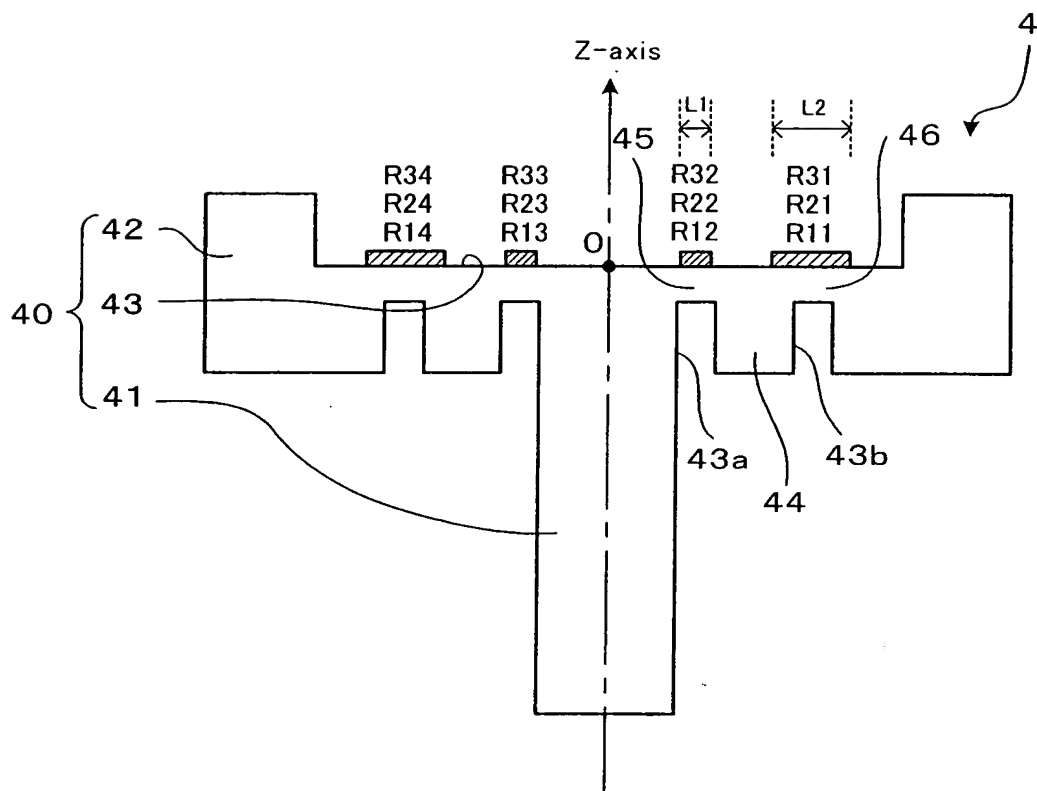


FIG. 9



A cross-sectional view of a semiconductor device 50 along the X-axis. The Z-axis is vertical, and the X-axis is horizontal. The origin 0 is at the center of the top surface. The device features a central trench 51. On the left side, there is a structure 52 with a top surface 53. A layer 54 is formed on the top surface 53, with regions 53a and 53b. On the right side, there is a structure 56 with a top surface 55. A layer 54 is also formed on the top surface 55, with regions 53a and 53b. The device includes four regions labeled R11, R12, R13, and R14, which are shaded with diagonal lines. The width of the trench 51 is labeled W1, and the width of the region 53a is labeled W2.

FIG. 11

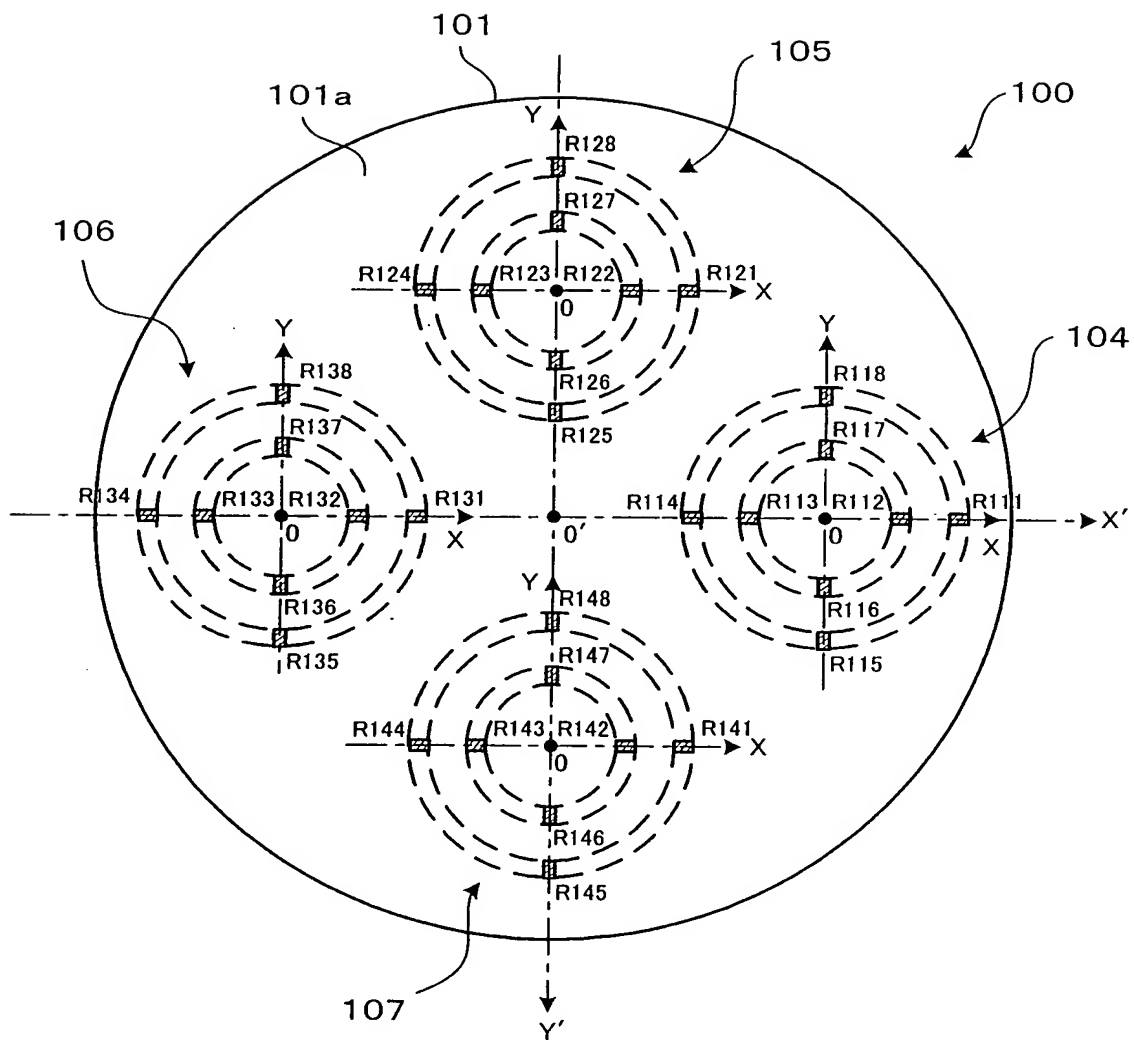


FIG. 12

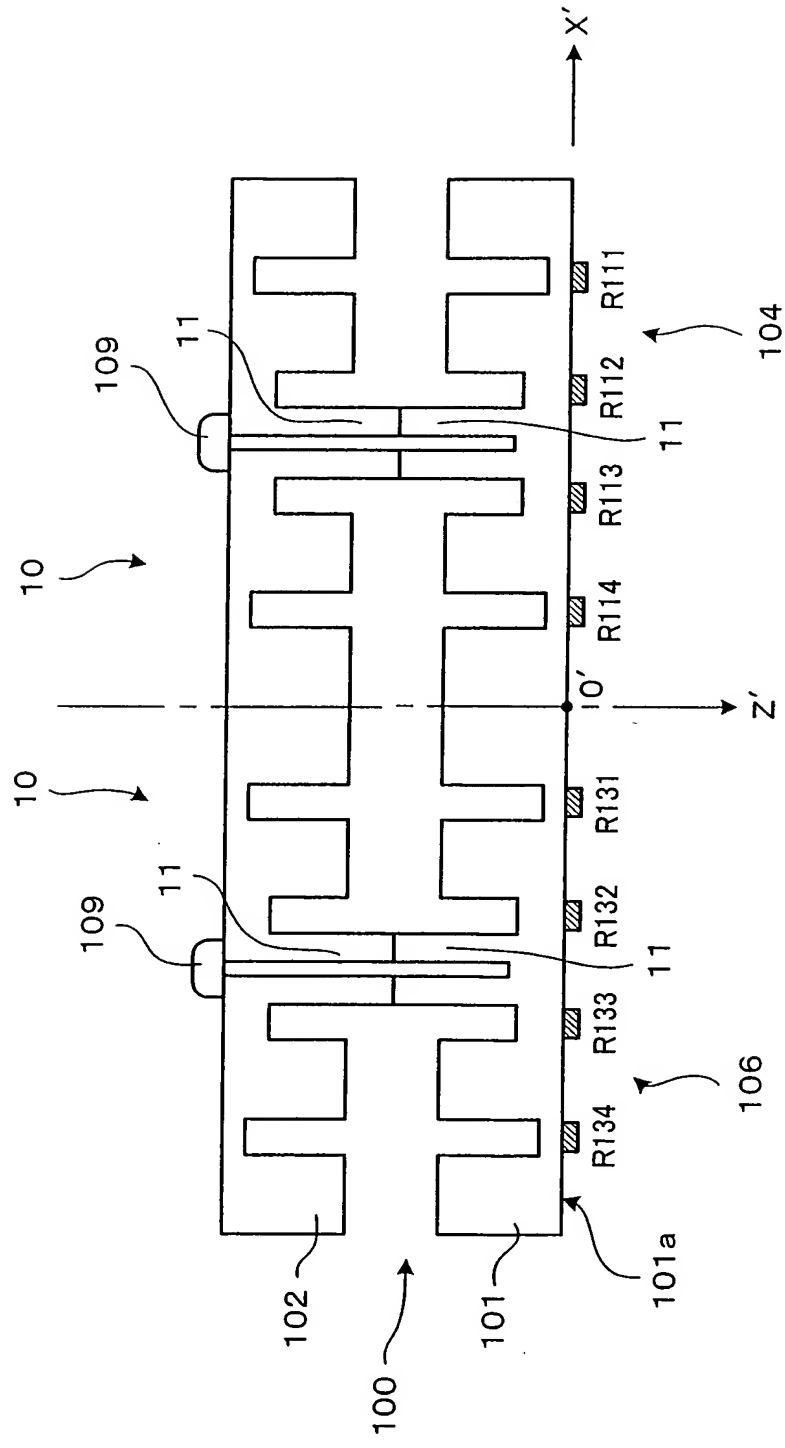


FIG. 13

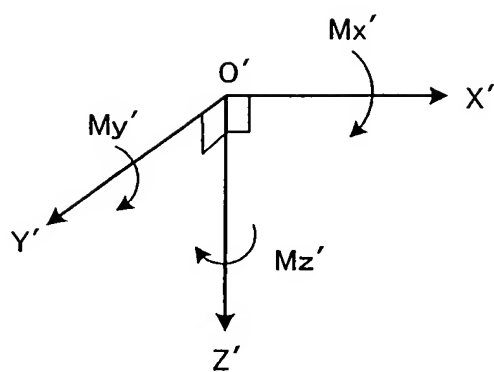


FIG. 14

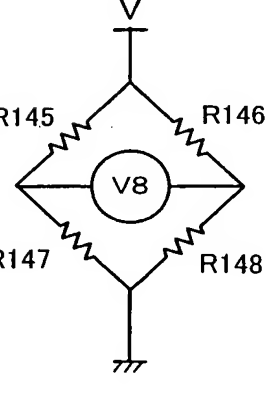
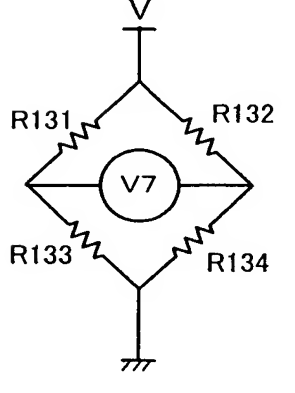
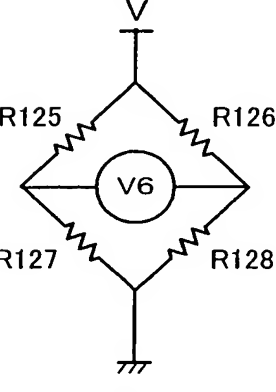
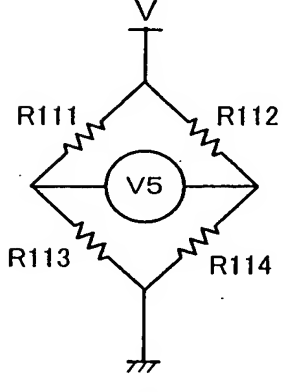
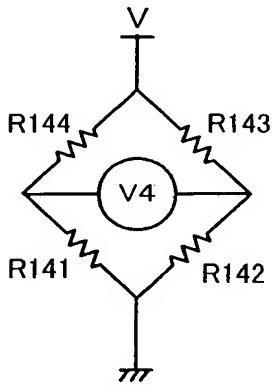
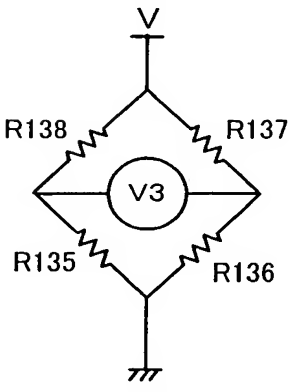
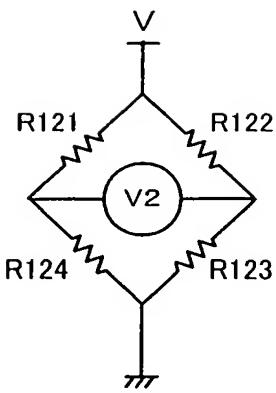
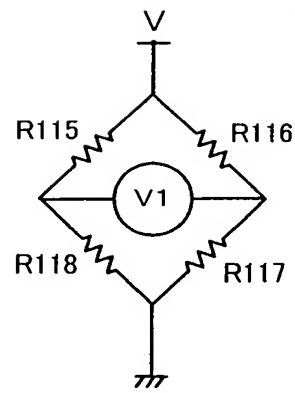


FIG. 15

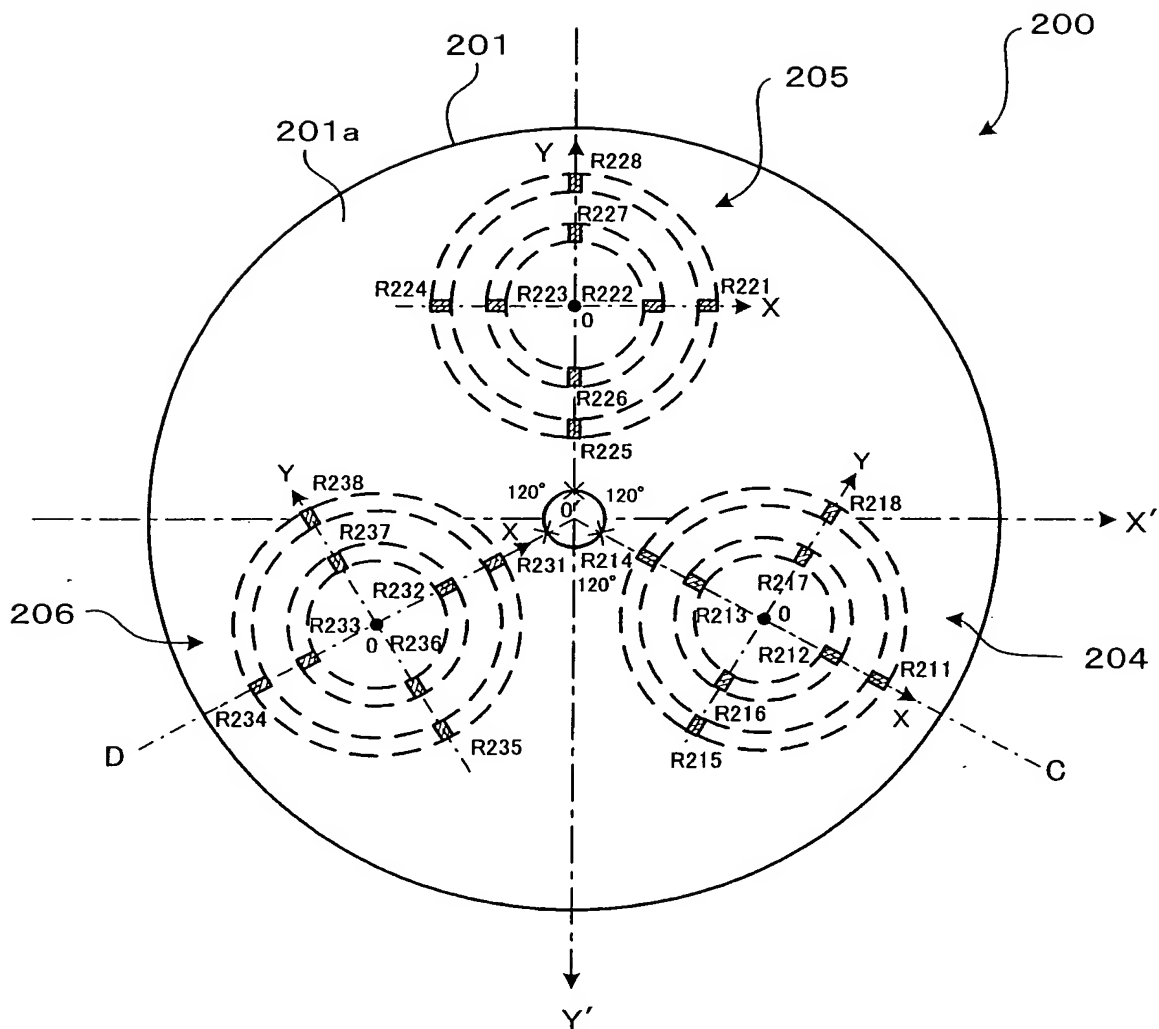




FIG. 16

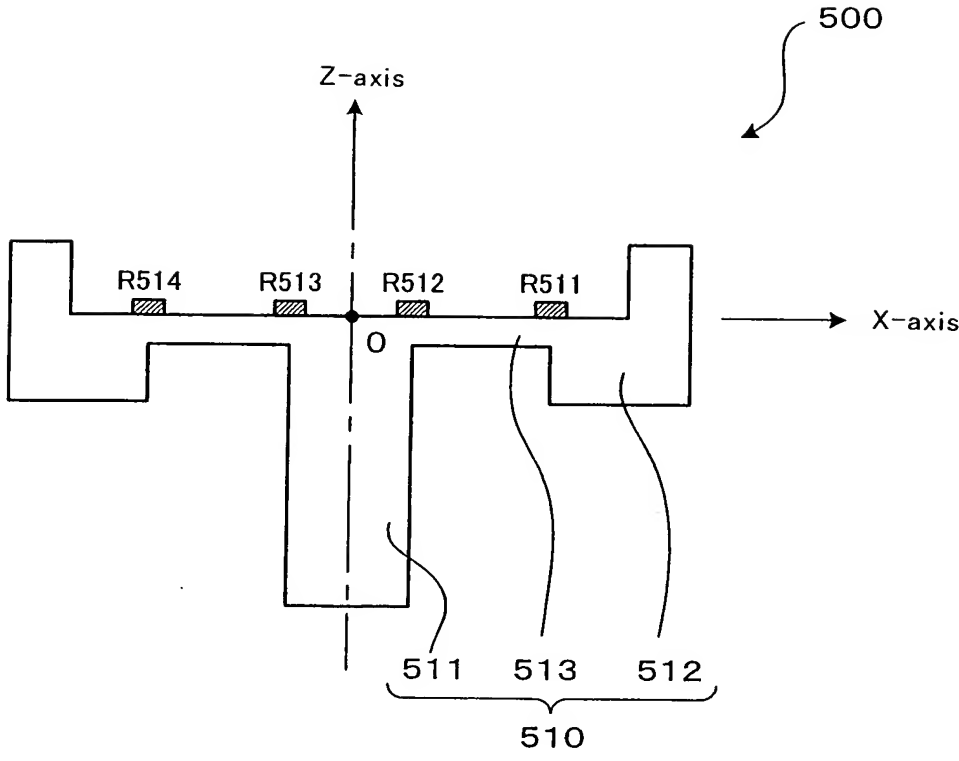


FIG. 17

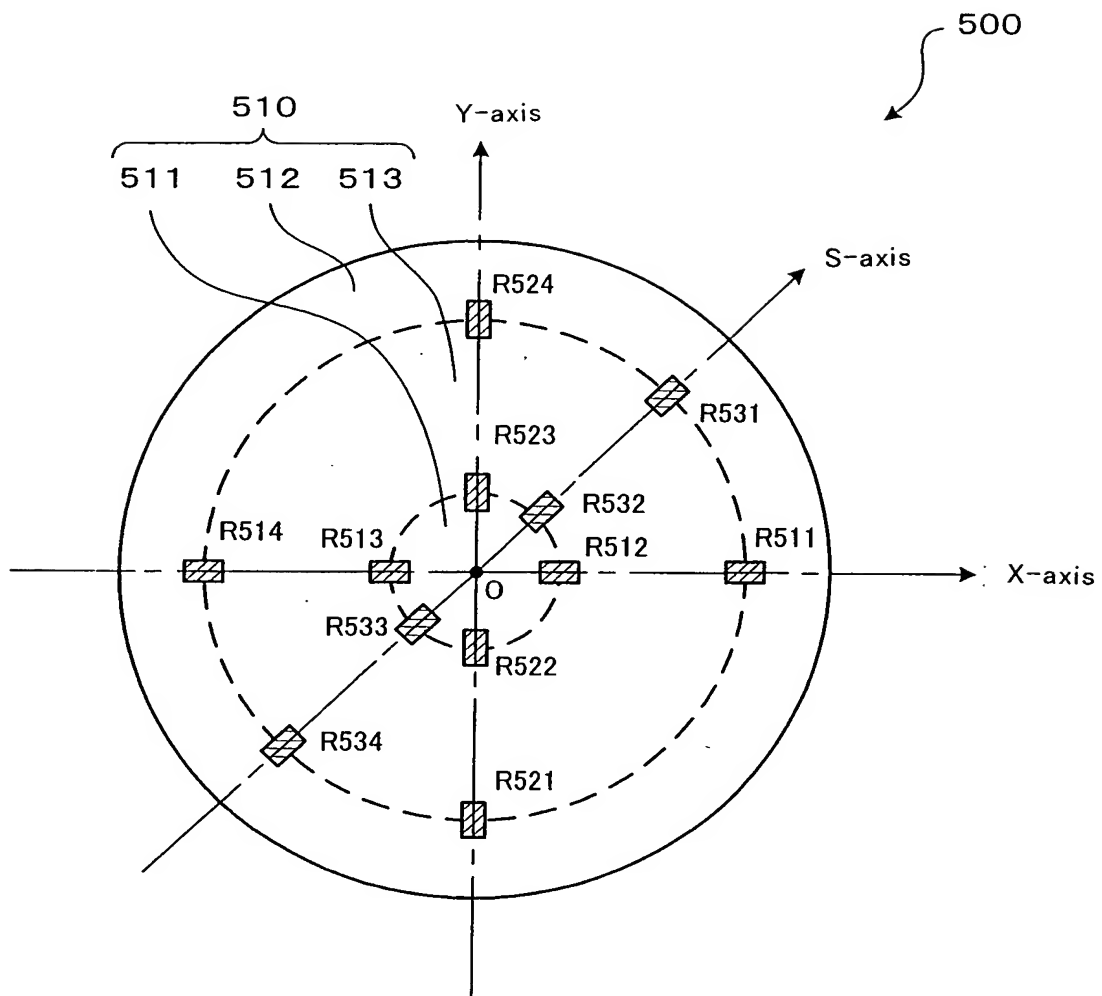


FIG. 18A

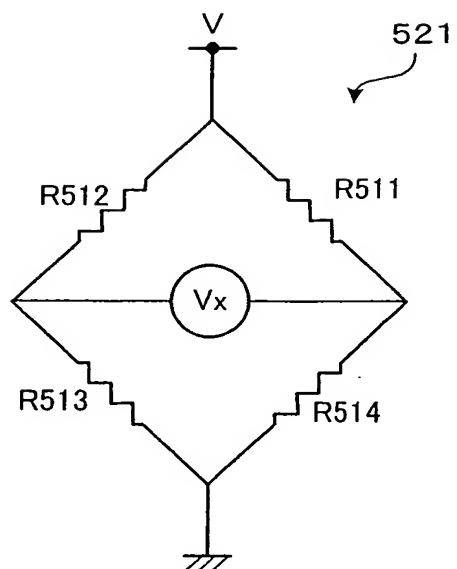


FIG. 18B

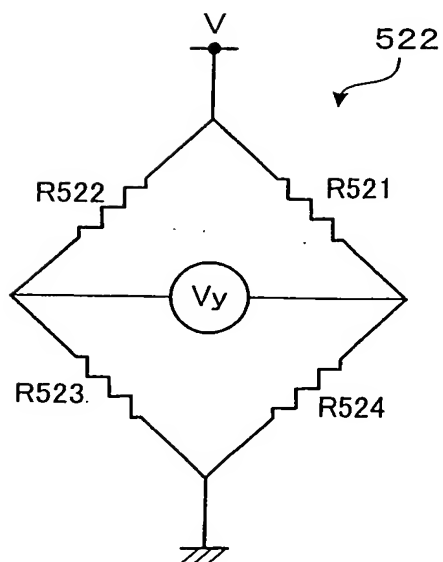


FIG. 18C

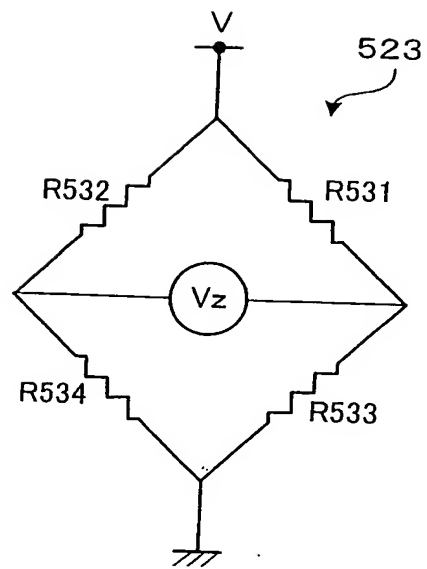


FIG. 19

